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| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 10/685,569  | 10/16/2003  | Beom-Jun Jin         | SEC.872D            | 7173             |
| 20987   | 7590        | 01/04/2005           | EXAMINER            |                  |
| VOLENTINE FRANCOS, & WHITT PLLC<br>ONE FREEDOM SQUARE<br>11951 FREEDOM DRIVE SUITE 1260<br>RESTON, VA 20190 |             |                      | WILSON, SCOTT R     |                  |
|   |             |                      | ART UNIT            | PAPER NUMBER     |
|   |             |                      | 2826                |                  |

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |                                      |                                   |  |
|------------------------------|--------------------------------------|-----------------------------------|--|
| <b>Office Action Summary</b> | <b>Application No.</b><br>10/685,569 | <b>Applicant(s)</b><br>JIN ET AL. |  |
|                              | <b>Examiner</b><br>Scott R. Wilson   | <b>Art Unit</b><br>2826           |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 08 October 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 14-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 14-18 is/are rejected.
- 7) ☒ Claim(s) 19 and 20 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 14-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Graettinger et al.. As to claim 14, Graettinger et al., Figure 14, discloses a method for fabricating a semiconductor memory device comprising: forming a pad (1100) on a semiconductor substrate (110); forming an interlayer dielectric layer (400) on the pad and semiconductor substrate for insulating the pad; forming a bit line stack (120), which includes bit line spacers (Figure 2, element 130), on the interlayer dielectric layer; forming a pair of bit line spacers at both side walls of the bit line stack; forming a storage node contact hole (850) in the interlayer dielectric layer using a self align contact etching method, the storage node contact hole being aligned at the bit line spacers and exposing the pad; and forming a multi-layered storage node contact plug in the storage node contact hole, by sequentially forming a first storage node contact plug (1200) and a second node contact plug (610) in the storage node contact hole.

As to claim 15, Graettinger et al. discloses (col. 7, lines 40-44) that the first storage node contact plug (1200) is formed of titanium nitride and the second storage node contact plug (610) is formed from polysilicon (col. 5, lines 32-33).

As to claim 16, Graettinger et al., Figure 14, discloses (col. 5, lines 54-55) a barrier metal layer (800) formed on the second storage node contact plug, wherein the barrier metal layer functions as a third storage node contact plug (col. 5, line 64).

As to claim 17, Graettinger et al. discloses (col. 5, line 55) that the barrier metal layer is formed from titanium nitride.

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As to claim 18, Graettinger et al. discloses that the formation of the multi-layered storage node contact plug comprises: forming a first storage node contact plug material layer (1200) on an entire surface of the semiconductor substrate after the storage node contact hole is formed, thereby partially filling the storage node contact hole; forming a second storage node contact plug material layer (610) on the first storage node contact plug material layer to sufficiently fill the storage node contact hole; forming a second storage node contact plug in the storage node contact hole by etching back the second storage node contact plug material layer; forming a barrier metal material layer (800) on the entire surface of the semiconductor substrate on which the second storage node contact plug is formed; and etching the first storage node contact plug material layer and the barrier metal material layer on the bit line stack.

***Allowable Subject Matter***

Claims 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed multi-layer contact plug with an ohmic contact layer formed under the first contact plug.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

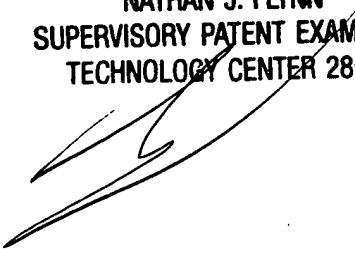
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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srw

December 23, 2004

**NATHAN J. FLYNN**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**

A handwritten signature in black ink, appearing to be 'Nathan J. Flynn', is written over the printed name and title.